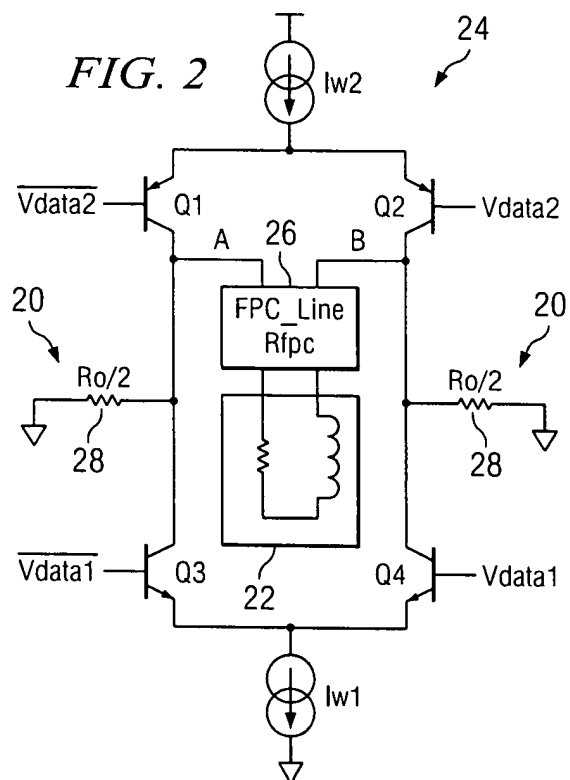
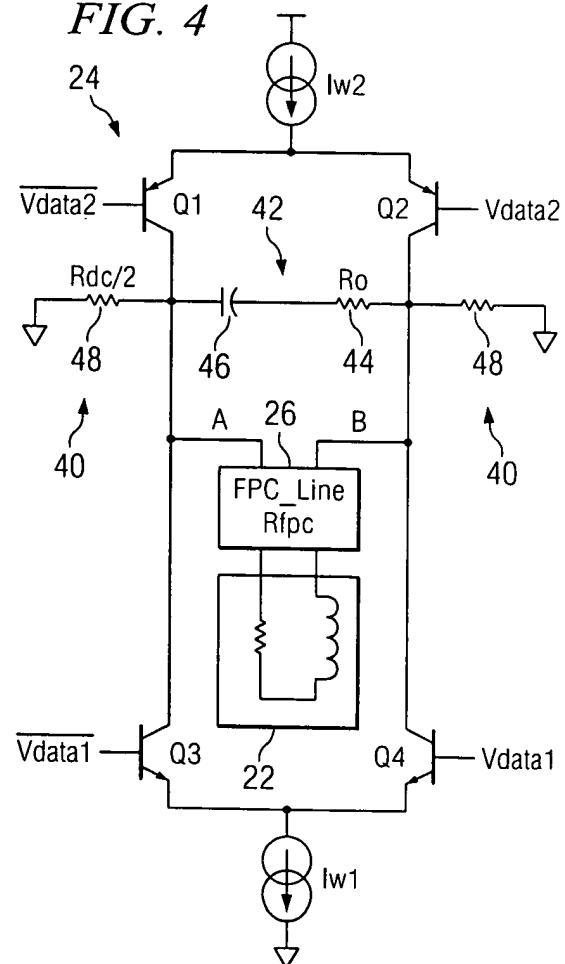


The diagram shows a differential pair of transistors on the left and another differential pair on the right. The gates of the left pair are connected to a common input signal 'Vdata'. The gates of the right pair are connected to a common input signal 'Vdata'. The drains of the left pair are connected to a central load consisting of an inductor and a resistor in parallel. The load is labeled 'FPC_Line Ripc' and 'wR-HEAD Lh, Rh'. The drains of the right pair are also connected to this central load. The sources of all transistors are connected to ground.



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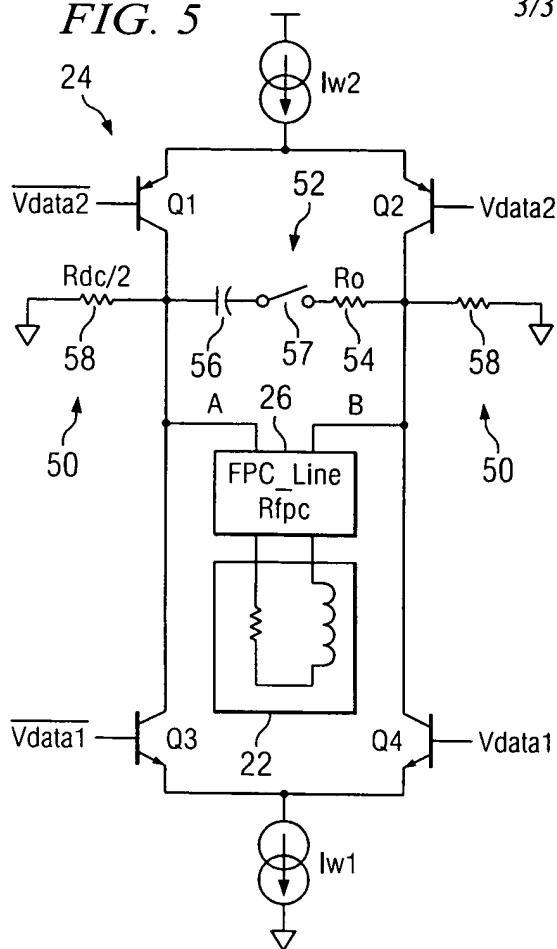


FIG. 6

